Low Voltage Intel® Pentium® III Processor 512K Dual Processor Platform

Design Guide

March 2002

Order Number: 273674-001

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Revision History

Date	Revision	Description
March 2002	001	First release of this document.

1.0 Introduction

This design guide is intended to be used by LV Intel Pentium III processor 512K system developers. This design guide documents Intel's design recommendations for dual-processor systems based on the LV Intel® Pentium® III processor 512K with the ServerWorks* HE-SL and LE3 chipset. In addition to providing design recommendations such as layout and routing guidelines, this document also addresses possible system design issues such as processor power delivery, layout considerations for mechanical pieces, EMI design impacts and system bus decoupling.

Carefully follow the design information, debug recommendations and system checklist presented in this document. These design guidelines have been developed to ensure maximum flexibility for board designers while reducing the risk of board related issues. The design information provided in this document falls into one of two categories:

- **Design Recommendations** are necessary to meet the timing and signal quality specifications.
- **Design Considerations** are suggestions for platform design. These provide one way to meet the design recommendations. They are based on the reference platforms designed by Intel. They could be used as an example, but may not be applicable to your particular design.

Note: The guidelines recommended in this document are based on experience and simulation work done at Intel while developing LV Intel Pentium III processor 512K based systems. The recommendations are subject to change.

1.1 Related Documents

The reader of this specification should also be familiar with the material and concepts presented in the following documents:

Table 1. Related Documents

Document	Order Number
P6 Family of Processors Hardware Developer's Manual	244001
IA-32 Intel® Architecture Software Developer's Manual • *Volume I: Basic Architecture* • *Volume II: Instruction Set Reference* • *Volume III: System Programming Guide*	 245470 245471 245472
VRM 8.5 DC-DC Converter Design Guidelines	249659
Low Voltage Intel® Pentium® III Processor 512K Datasheet	273673
Low Voltage Intel® Pentium® III Processor 512K (DP) Thermal Design Guide	273675
Low Voltage Intel® Pentium® III Processor 512K/815E Chipset Platform Design Guide	273676
Intel® Pentium® III Processor Specification Update	244453
Intel Processor Identification and the CPUID Instruction	241618

1.2 Conventions and Terminology

For this document, the following terminology applies.

- **Low Voltage Intel® Pentium® III Processor 512K** - Intel's name for the next generation Intel® Pentium® III processor based on Intel's 0.13-micron (i.e., 1.25 V V_{TT} / AGTL) technology. This processor contains 512 Kbytes of L2 cache, is dual processor capable, and has a 133 MHz processor side bus.
- **Micro FCBGA** - Micro Flip Chip Ball Grid Array. The package technology used on the LV Intel Pentium III processor 512K.
- **Keep-out zone** - The area on or near a Micro FCBGA packaged processor that system designs can not utilize.
- **Processor** - For this document, the term processor is the generic form of the LV Intel Pentium III processor 512K for the Micro FCBGA package.

2.0 General Design Considerations

This section documents layout and routing guidelines for LV Intel Pentium III processor 512K platforms. This section does not discuss the functional aspects of any bus, or the layout guidelines for an add-in device.

If the guidelines listed in this document are not followed, it is very important that thorough signal integrity and timing simulations are completed for each design. Any deviation from the guidelines should be simulated. Even when the guidelines are followed, Intel recommends that you simulate critical signals to ensure proper signal integrity and flight time.

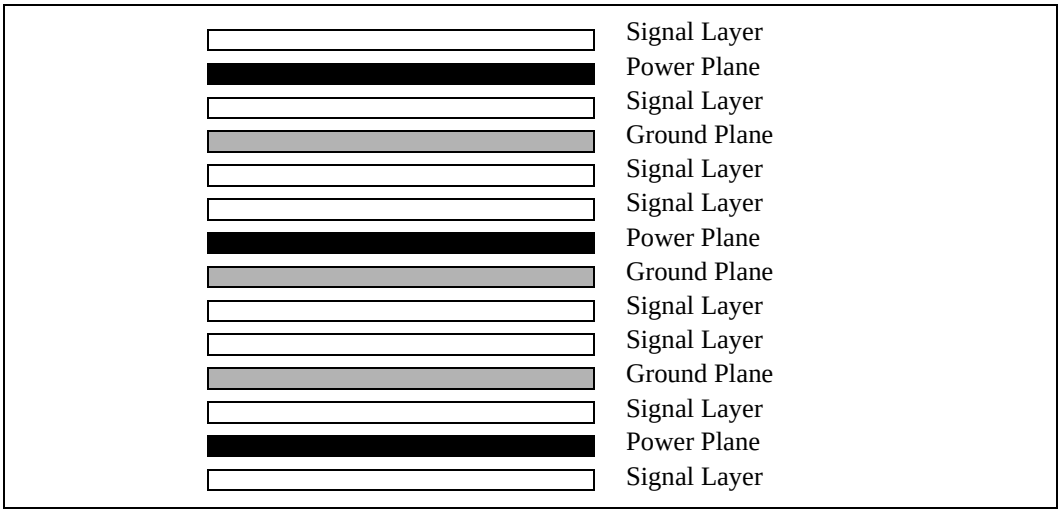
The trace impedance noted (i.e., 55 Ω ± 10%) is the "nominal" trace impedance for a 4.5-mil wide trace. Nominal trace impedance is the impedance of the trace when not subjected to the fields created by changing current in neighboring traces. When calculating flight times, it is important to consider the minimum and maximum impedance of a trace based on the switching of neighboring traces. Using wider spaces between the traces can minimize this trace-to-trace coupling. In addition, these wider spaces reduce settling time.

Coupling between two traces is a function of the coupled length, the distance separating the traces, the signal edge rate, and the degree of mutual capacitance and inductance. To minimize the effects of trace-to-trace coupling, follow the routing guidelines documented in this section.

2.1 Nominal Board Stackup

Figure 1 is an example of a 14-layer board stack-up. The impedance of all the signal layers should be 55 Ω ± 10%. A lower trace impedance reduces signal edge rates, overshoot, and undershoot, and has less crosstalk than a higher trace impedance. A higher trace impedance increases edge rates and may slightly decrease signal flight times. Please note that thicker core may help reduce board warpage issues.

Figure 1. Sample Board Stackup



Additional guidelines on board stack-up, placement, and layout include the following.

- The board impedance (Z) should be between 49.5 Ω and 60.5 Ω (55 Ω ± 10% is recommended).
- The dielectric process variation in the PCB fabrication should be minimized.
- The ground plane should not be split on the ground plane layer.
- Keep vias for decoupling capacitors as close to the capacitor pads as possible.

2.2 Micro-FCBGA Component Keepout

Figure 2 shows the keepout zones and dimensions for the Micro-FCBGA package. Table 2 provides the values for the mechanical specifications.

Figure 2. Micro-FCBGA Component Keepout

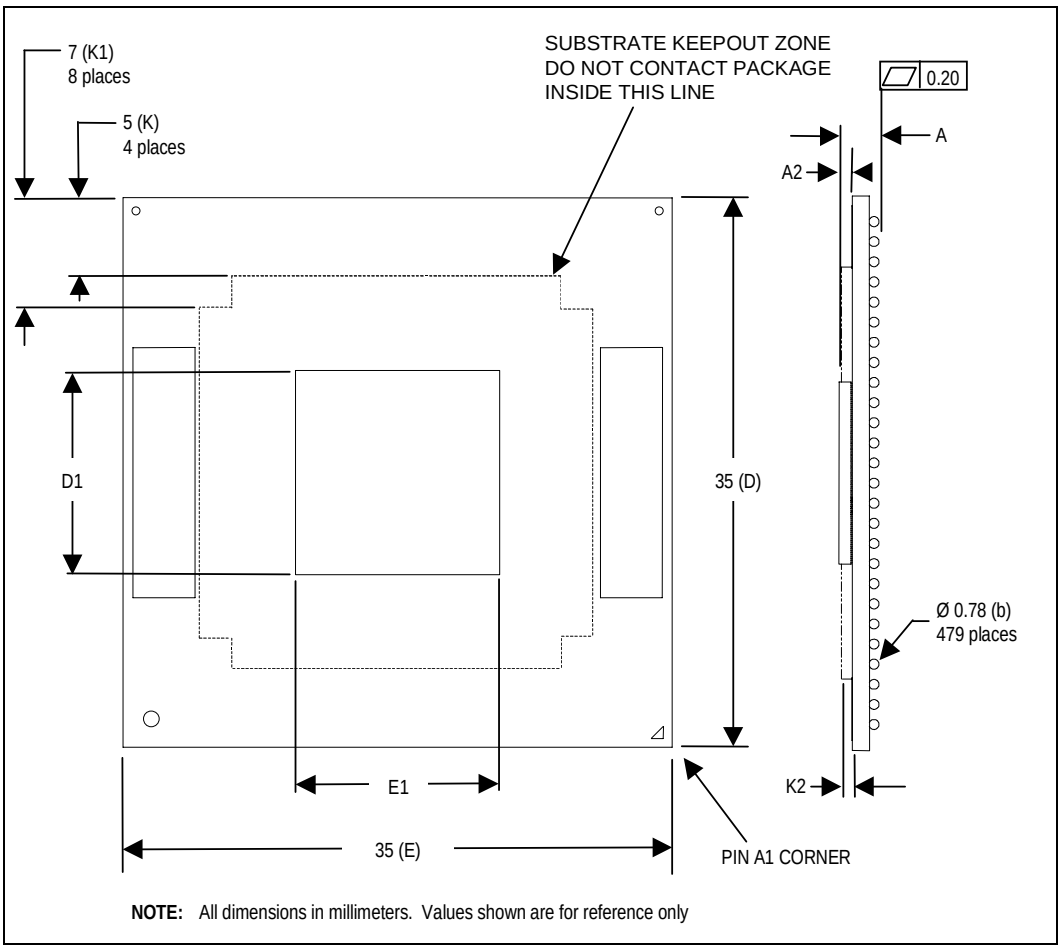
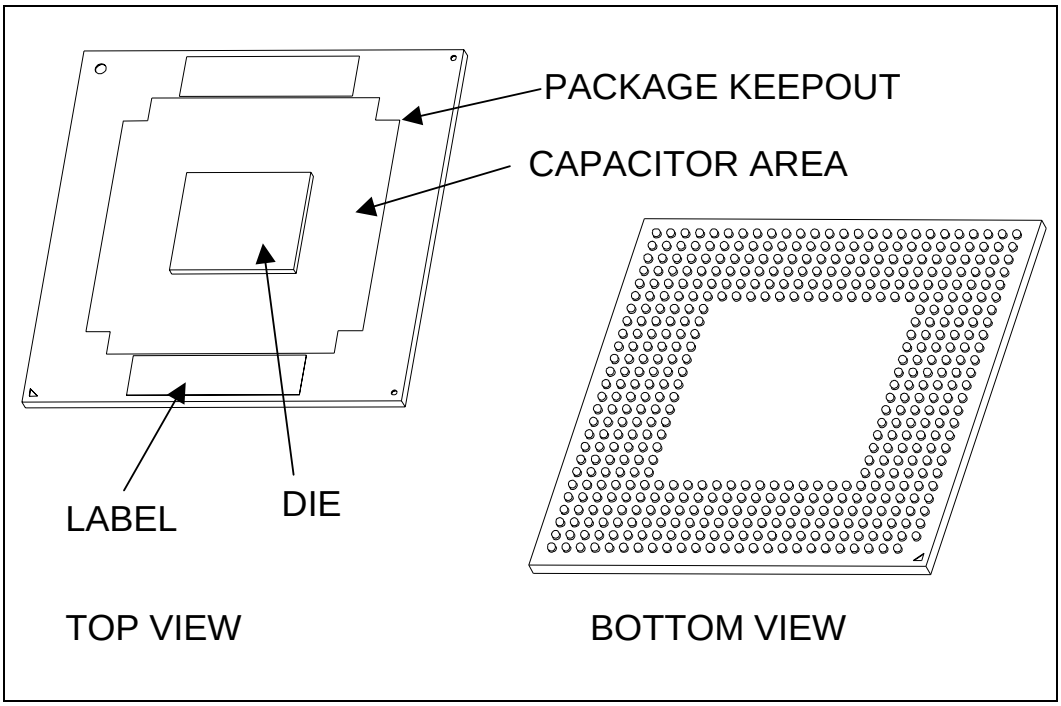


Table 2. Micro-FCBGA Package Mechanical Specifications

Symbol	Parameter	Min	Max	Unit
A	Overall height, as delivered (1)	2.27	2.77	mm
A2	Die height	0.854		mm
b	Ball diameter	0.78		mm
D	Package substrate length	34.9	35.1	mm
E	Package substrate width	34.9	35.1	mm
D1	Die length	11.18		mm
E1	Die width	7.19		mm
e	Ball pitch	1.27		mm
N	Ball count	479		each
K	Keep-out outline from edge of package	5		mm
K1	Keep-out outline at corner of package	7		mm
K2	Capacitor keep-out height	—	0.7	mm
S	Package edge to first ball center	1.625		mm
--	Solder ball coplanarity	0.2		mm
Pdie	Allowable pressure on the die for thermal solution	—	689	kPa
W	Package weight	4.5		g

NOTES:
1. All dimensions are subject to change.
2. Overall height as delivered. Values were based on design specifications and tolerances. Final height after surface mount depends on OEM motherboard design and SMT process.

Figure 3. Micro-FCBGA Package – Top and Bottom Isometric Views



3.0 Processor Host Bus Design

3.1 Initial Timing Analysis

To determine the available flight time window, perform an initial timing analysis. Analysis of setup and hold conditions will determine the minimum and maximum flight time bounds for the system bus. Use the following equations to establish the system flight time limits.

Table 3. System Timing Equations

Equation
$T_{flight,min} >= T_{hold} - T_{co,min} + T_{skew}$
$T_{flight,max} <= T_{cycle} - T_{co,max} - T_{su} - T_{skew} - T_{jit} - T_{adj}$

Table 4. System Timing Terms

Term	Description
T_{cycle}	System cycle time. Defined as the reciprocal of the frequency.
$T_{flight,min}$	Minimum system flight time.
$T_{flight,max}$	Maximum system flight time.
$T_{co,max}$	Maximum driver delay from input clock to output data.
$T_{co,min}$	Minimum driver delay from input clock to output data.
T_{su}	Minimum setup time. Defined as the time for which the input data must be valid prior to the input clock.
T_{hold}	Minimum hold time. Defined as the time for which the input data must remain valid after the input clock.
T_{skew}	Clock generator skew. Defined as the maximum delay variation between output clock signals from the system clock generator, the maximum delay variation between clock signals due to system board variation and chipset loading variation.
T_{jit}	Clock jitter. Defined as the maximum edge to edge variation in a given clock signal.
T_{adj}	Multi-bit timing adjustment factor. This term accounts for the additional delay that occurs in the network when multiple data bits switch in the same cycle. The adjustment factor includes mechanisms such as package and PCB crosstalk, high inductance current return paths, and simultaneous switching noise.

Component timings for the LV Intel Pentium III processor 512K are available in the *Low Voltage Intel® Pentium® III Processor 512K Datasheet* (order number 273673). Please contact your chipset vendor for documentation concerning the chipset component timing.

Table 5 provides recommended values for system timings. Skew and jitter values for the clock generator device come from the clock driver vendor's datasheet. The PCB skew specification is based on the results of extensive simulations performed by Intel engineers. The T_{adj} value is based on Intel's experience with systems that use previous generations of processors.

Table 5. System Bus Timing Parameters

Timing Term	Value
T_{skew} [ns]	0.25
T_{jit} [ns]	0.20
T_{adj} [ns]	0.50
T_{cycle} [ns] (133 MHz)	7.50

Table 6 summarizes the flight time requirements for CPU to CPU transfers that result from using the component timing specifications and recommended system timings. All component values should be verified against the latest specifications before proceeding with analysis.

Table 6. Sample CPU to CPU flight time calculations

Driver	Receiver	Calculation
CPU	CPU	$T_{flight,min}$ >= 1.0 - 0.4 + 0.25 = 0.85 ns
CPU	CPU	$T_{flight,max}$ <= 7.5 - 3.25 - 0.95 - 0.25 - 0.2 - 0.5 = 2.35 ns

3.2 General Topology and Layout Guidelines

Intel recommends that all LV Intel Pentium III processor 512K dual-processing platforms use a system bus T-topology. Figure 4 shows a high level diagram of this topology. The pull-up resistors shown inside the processor packages are the processor's on-die AGTL termination, since the LV Intel Pentium III processor 512K has on-die termination.

Figure 4. System Bus T-Topology

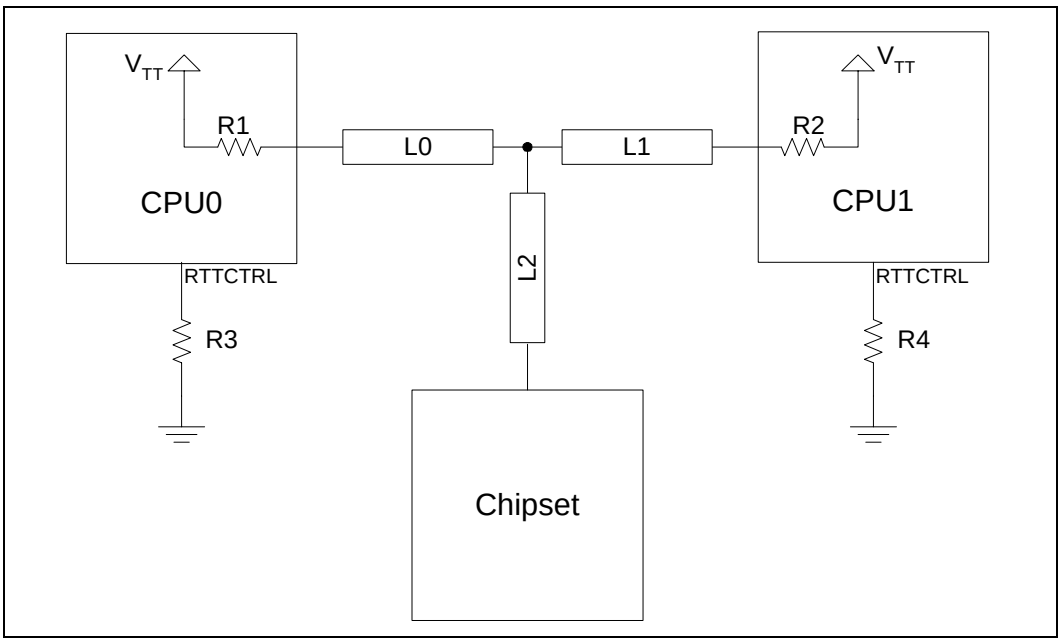


Table 7 contains the length specifications for the segments of the T-topology. Note that lengths L0 and L1 must be length matched to within 0.25 inches (per net, not between nets). Table 8 contains the component values for the T-topology.

Table 7. Trace Lengths for "T" Topology (ServerWorks Chipset)

Segment	Min Length (inches)	Max Length (inches)
L0	2.8	3.4
L1	2.8	3.4
L2	1.7	2.3

Table 8. Component Values for T Topology

Reference	Value	Tolerance
R1 (on chip)	R3	N/A
R2 (on chip)	R4	N/A
R3	68Ω	+/- 10%
R4	68Ω	+/- 10%

3.3 Wired-OR Signal Considerations

The Wired-OR signals of the processor's host bus require additional consideration. The Wired-OR signals in a LV Intel Pentium III processor 512K processor system are HIT#, HITM#, BNR#, AERR#, BERR#, and BINIT#. The Wired-OR signals may be driven by multiple bus agents at the same time, such as both processors asserting the HIT# signal to signify a cache hit on a line they both contain. With multiple driving agents, these signals are susceptible to being overdriven, which results in excessive overshoot and ringback on these signals.

Terminating the Wired-OR signals at the chipset branch of the T topology reduces the effect of multiple driving agents on these signals. Intel recommends that system designers carefully examine the signal integrity of these signals and optionally implement the circuit shown in Figure 5. This recommendation will work correctly for systems designed with the standard T topology.

Please note that the incorporation of Wired-OR termination is optional. Intel has not seen any system failures on systems which do not implement the Wired-OR termination recommendations. Therefore, systems which are already in the latter phases of design may wish to forgo implementing these recommendations until an opportunity presents itself to incorporate them. However, it is the responsibility of the system designer to ensure that the signal quality of these signals meets the component specifications.

Figure 5. Wired-OR Termination Topology

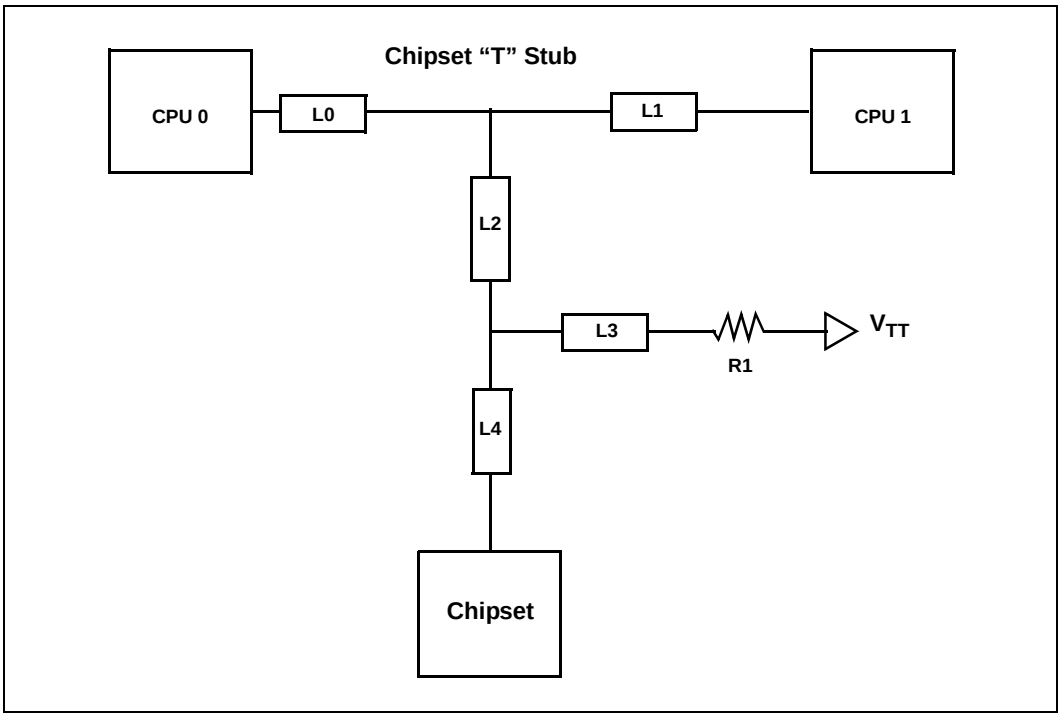


Table 9. Wired-OR Values

Item	Min	Max	Notes
L0	2.8"	3.4"	
L1	2.8"	3.4"	
L2	1.70"	2.3"	
L3		1.5"	Route to shortest length
L4	0"	0.2"	Should be as short as possible. Optimal case is to make this value zero, making the L3 stub come after the chipset pin.
R1	100 Ω	220 Ω	The range of values has tradeoffs in flight time and dampening effects. 150 Ω ±10% is a base recommendation.

Please note that the value range for R1 present a set of tradeoffs for flight time and dampening effects. Choosing a value near the upper end of the range (around 200 Ω) impacts the flight times the least, but provides minimal dampening. Choosing a value at the lower end of the range (around 100 Ω), provides optimal dampening but has a larger impact on the signal flight times. Intel recommends a value of 150 Ω ±10% as a reasonable tradeoff between dampening and flight time.

3.4 Simulation Methodology

Analog simulations are recommended for high-speed system bus designs. Start simulations prior to layout. Pre-layout simulations provide a detailed picture of the working "solution space" that meets flight time and signal quality requirements. By basing board layout guidelines on the solution space, the iterations between layout and post-layout simulations can be reduced.

Intel recommends running simulations at the device pads for signal quality and at the device pins for timing analysis. However, simulation results at the device pins may be used later to correlate simulation performance against actual system measurements.

The *Low Voltage Intel® Pentium® III Processor 512K I/O Signal Integrity Models* are available from http://www.intel.com/design/pentiumiii/devtools.

3.5 Trace Routing

The following guidelines should be followed when routing the AGTL host bus signal traces:

- Traces should have an impedance of 55 Ω ± 10%
- The nominal trace width should be 4.5 mils.
- The L0 and L1 lengths in Table 7 should be matched to within 0.25 inches (per net, not between nets).
- Minimize the number of vias and layer transitions.
- Minimum 10 mils spacing

3.6 Layout Rules for AGTL Signals

3.6.1 Ground Reference

It is strongly recommended that AGTL signals be routed on the signal layer next to the ground layer (referenced to ground). It is important to provide effective signal return path with low inductance. The best signal routing is directly adjacent to a solid GND plane with no splits or cuts. Eliminate parallel traces between layers not separated by a power or ground plane.

3.6.2 Reference Plane Splits

Splits in reference planes disrupt signal return paths and increase overshoot/undershoot due to significantly increased inductance. For optimal signal integrity, high-speed signals should not be routed over power plane splits.

3.6.3 CPU Breakout

Intel strongly recommends that AGTL signals do not traverse multiple signal layers. Intel recommends breaking out all signals from the CPU on the same layer. If routing is tight, breakout from the CPU on the opposite routing layer over a ground reference, and cross over to the main signal layer near the CPU.

Note: Following the above layout rules is critical for AGTL signal integrity.

3.6.4 Minimizing Crosstalk

Adhering to the following general rules will minimize the impact of crosstalk in the high speed AGTL bus design:

- Maximize the space between traces. Maintain a minimum of 10 mils (assuming a 4.5 mil trace) between trace edges wherever possible. It may be necessary to use tighter spacing when

routing between component pins. Minimize the distance that traces have to be close and parallel to each other, and maximize the distance between the sections when the spacing restrictions relax.

- Avoid parallelism between signals on adjacent layers if there is no AC reference plane between them. As a rule of thumb, route adjacent layers orthogonally.
- Since AGTL is a low signal swing technology, it is important to isolate AGTL signals from other signals by at least 25 mils. This will avoid coupling from signals that have larger voltage swings, such as 3.3 V system memory.
- Select a board stack-up that minimizes the coupling between adjacent signals. Minimize the nominal characteristic impedance within the AGTL specification. This can be done by minimizing the height of the trace from its reference plane, which minimizes the crosstalk.
- Route AGTL address, data and control signals in separate groups to minimize crosstalk between groups. Keep at least 25 mils between each group of signals.
- Minimize the dielectric used in the system. This places the traces closer to their reference plane and reduces the crosstalk magnitude.
- Minimize the dielectric process variation used in the PCB fabrication.
- Minimize the cross sectional area of the traces. This can be done by using narrower traces or by using thinner copper, but the trade-off for this smaller cross sectional area is a higher trace resistivity that can reduce the falling edge noise margin because of the I*R loss along the trace.

3.7 Layout Rules for Non-AGTL (CMOS) Signals

The following layout rules should be used for all CMOS signals:

- The trace impedance should be 55 Ω +/- 10%.
- External termination resistors should be placed in the middle of the trace to prevent long reflection times and reduce reflection ledges.
- Do not route CMOS traces next to AGTL traces. Switching noise on the AGTL traces may attack the nearby CMOS traces.
- Route a CMOS trace on one signal layer. If layer switching is unavoidable, minimize the number of layer switches.
- Try to use only one reference plane for a trace (either Vcc or Vss).
- Although CMOS signals are slow, they may still have speed path problems. This is especially true for APIC clock and APIC data. Try to avoid long routes.

3.8 Undershoot/Overshoot Requirements

Overshoot (or undershoot) is the absolute value of the maximum voltage above the nominal high voltage or below VSS. The overshoot guideline limits transitions beyond VCC or VSS due to the fast signal edge rates. The processor can be damaged by repeated overshoot events on buffers if the charge is large enough (i.e., if the overshoot is great enough). Determining the impact of an overshoot/undershoot condition requires knowledge of the magnitude, the pulse direction and the activity factor (AF). Permanent damage to the processor is the likely result of excessive overshoot/undershoot. Violating the overshoot/undershoot guideline makes satisfying the ringback specification difficult.

When performing simulations to determine impact of overshoot and undershoot, ESD diodes must be properly characterized. ESD protection diodes do not act as voltage clamps and will not provide overshoot or undershoot protection. ESD diodes modeled within Intel I/O buffer models do not clamp undershoot or overshoot and will yield correct simulation results. If other I/O buffer models are being used to characterize the LV Intel Pentium III processor 512K performance, care must be taken to ensure that ESD models do not clamp extreme voltage levels. Intel I/O buffer models also contain I/O capacitance characterization. Therefore, removing the ESD diodes from an I/O buffer model will impact results and may yield excessive overshoot/undershoot.

Refer to the latest *Low Voltage Intel® Pentium® III Processor 512K Datasheet* for detailed undershoot/overshoot requirements.

3.9 Debug Port Routing Guidelines

This chapter describes the processor debug port, in-target probe (ITP) platform design guidelines.

3.9.1 Target System Implementation

Follow the implementation guidelines provided in this section to help ensure a fully functional ITP debug system. These guidelines are preliminary, and additional changes may be required. The signals involved in the ITP debug system are high speed signals and must be routed with high speed design considerations in mind. The implementation offers flexibility in areas such as JTAG routing (i.e., scan chain), addition of non-ITP compliant parts, and clock rate. However, the implementation is not flexible in system and execution signal connections.

Intel uses an ITP for internal debug and system validation and recommends that all system designs include a debug port.

3.9.1.1 Signal Layout Guidelines

The debug port (Test Access Port) is part of the processor scan chain. It must be connected to the bus clock and system bus signals. This implies that the designer will place the Debug Port within 12 inches of the nearest processor.

There are three signal groups within the debug port, as described in the datasheet. Each group has a different set of layout requirements. The system signals are special ITP-specific signals and are both inputs and outputs. The JTAG signals are system resources and may be shared with local JTAG tools. Input and output signals are available. The execution signals are a combination of CMOS and AGTL level signals. They are both inputs and outputs to the ITP.

The ITP TCK and TMS signals must be routed with a maximum trace resistance of 2.0 ohm to reduce the amount of DC shifting on these signals. This is due to the small termination values that are recommended for these signals.

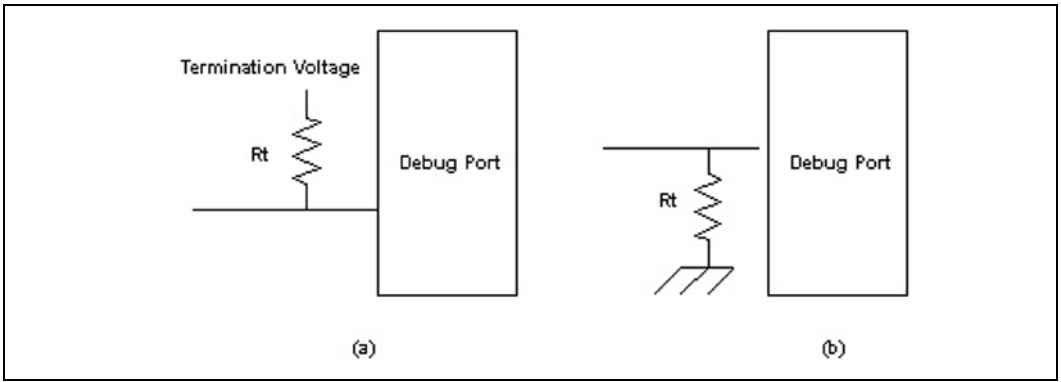
System Signal Layout Guidelines

Table 10 provides the system signal layout guidelines. See Table 13 for termination values.

Table 10. System Signal Layout Guidelines

Signal	Routing Notes	Sample Layout
POWERON	Route with normal trace 2 to 6 inches to the debug port connector	Figure 6a
BCLK, BCLK#		N/A
DBRESET#, BSEN#, DBINST#		Figure 6a

Figure 6. Simple Terminations



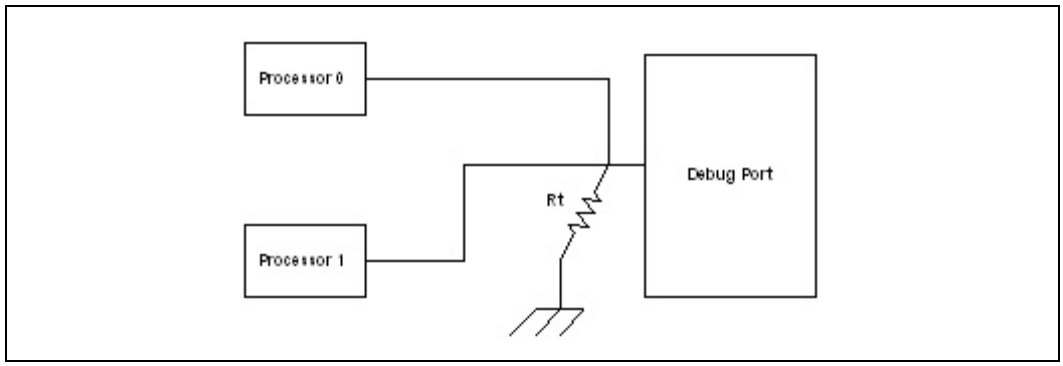
JTAG Signal Layout Guidelines

Reflections on TCK that cause mid-threshold ringing will render the primary system debug tool inoperative. Simulate the behavioral model, and verify signal integrity using your system bus signal analysis tools. The following table provides the JTAG signal layout guidelines. It is highly recommended that TCK be simulated to ensure proper signal quality is maintained.

Table 11. JTAG Signal Layout Guidelines

Signal	Routing Notes	Sample Layout
TCK	Critical JTAG signal which requires timing and signal integrity considerations; driver is 74VCX16245 with external edge rate control on TCK	Figure 7
TMS, TDI, TDO	Critical JTAG signal which requires timing and signal integrity considerations. ITP driver is 74VCX16245. TMS must be routed with TCK.	Figure 6a
TRST#	Pull-down resistors should be used to force TRST# assertion (low).	Figure 6b

Figure 7. TCK Termination, DP System



Execution Signal Layout Guidelines

Table 12. Execution Signals Routing Guidelines

Signal	Routing Notes	Sample Layout
PREQx#	AGTL signal routing guidelines apply	Figure 6 (a)
PRDYx#		Figure 8
RESET#	The flight time of the RESET# signal from the closest processor must be added to the arrival time of BCLK at the Debug Port.	Figure 9

Figure 8. PRDYx# Signal Termination

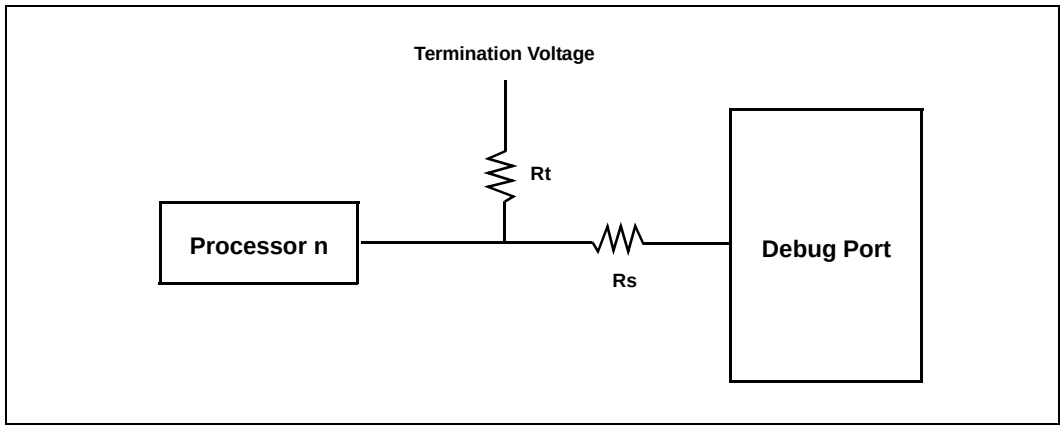
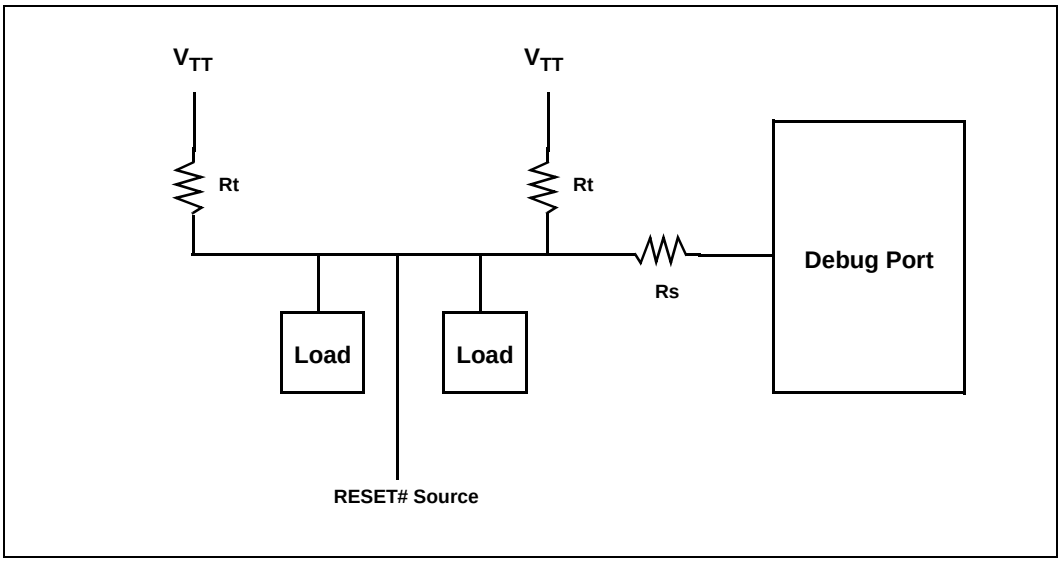


Figure 9. RESET# Signal Termination



3.9.1.2 Signal Termination Requirements

Table 13 lists signal termination requirements for the debug port signals.

Table 13. Debug Port Termination Requirement

Signal	Signal Termination Value (Rt)	Termination Value (Rs)	Termination Voltage (Rt)
System Signal			
POWERON	1.5 KΩ	N/A	V_{TT}
BCLK, BCLK#			
BSEN#	240 Ω	N/A	V_{CC}
DBRESET#	240 Ω	N/A	V_{CC}
DBINST#	10 KΩ	N/A	V_{CC}
JTAG Signals			
TCK	39 Ω	N/A	GND
TDI	200 - 300 Ω	N/A	V_{CC}CMOS
TDO	150 Ω	N/A	V_{CC}CMOS
TMS	39 Ω	N/A	V_{CC}CMOS
TRST#	500 - 680 Ω	N/A	GND
Execution signals			
RESET#	Match to AGTL characteristic impedance	240 Ω	V_{TT}
PREQx#	200 - 300 Ω	N/A	V_{CC}CMOS
PRDYx#	Match to AGTL characteristic impedance	240 Ω	V_{TT}

3.9.1.3 Routing Guidelines

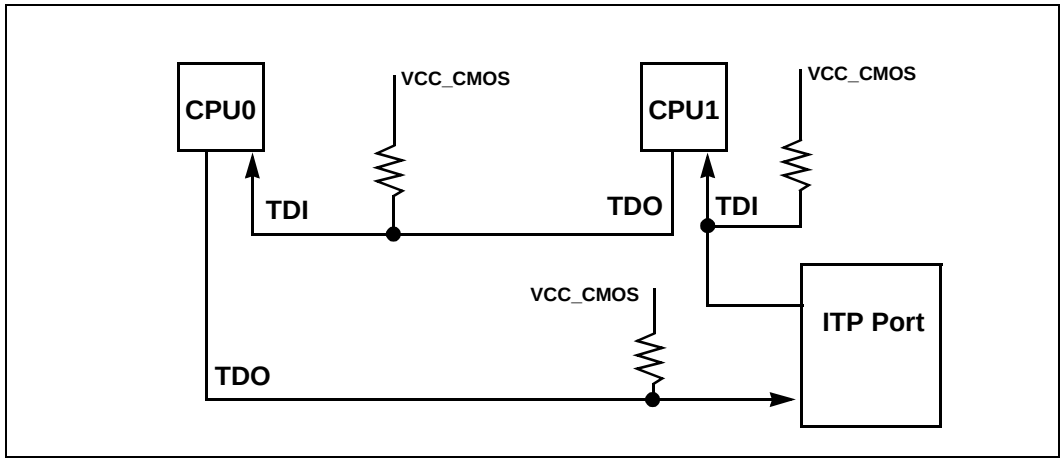
Table 14. Routing Guidelines

Parameter	Reference Figure	Description
TCK	Figure 7	1" max from debug port to RT AND 12" max from debug port to processor VERY SENSITIVE TO NOISE -- please route accordingly
TMS, TDO, TDI, POWERON, DBRESET#, BSEN#, DBINST#, PREQx#	Figure 6 (a)	1" max from debug port to RT AND 12" max from debug port to processor
TRST#	Figure 6 (b)	1" max from debug port to RT AND 12" max from debug port to processor
PRDYx#	Figure 8	1" max from debug port to RS AND 1" max from debug port to RT AND 12" max from debug port to processor (AGTL guidelines)
RESET#	Figure 9	1" max from debug port to RS AND 1" max from debug port to RT AND 12" max from debug port to processor

3.9.1.4 System Implementation

Figure 10 demonstrates the expected route of the JTAG data link for a processor only cluster. It is obligatory to pull up TDI/TDO for each signal.

Figure 10. JTAG Signals TDI/TDO for Processor Only



4.0 Clocking

4.1 General Clocking Considerations

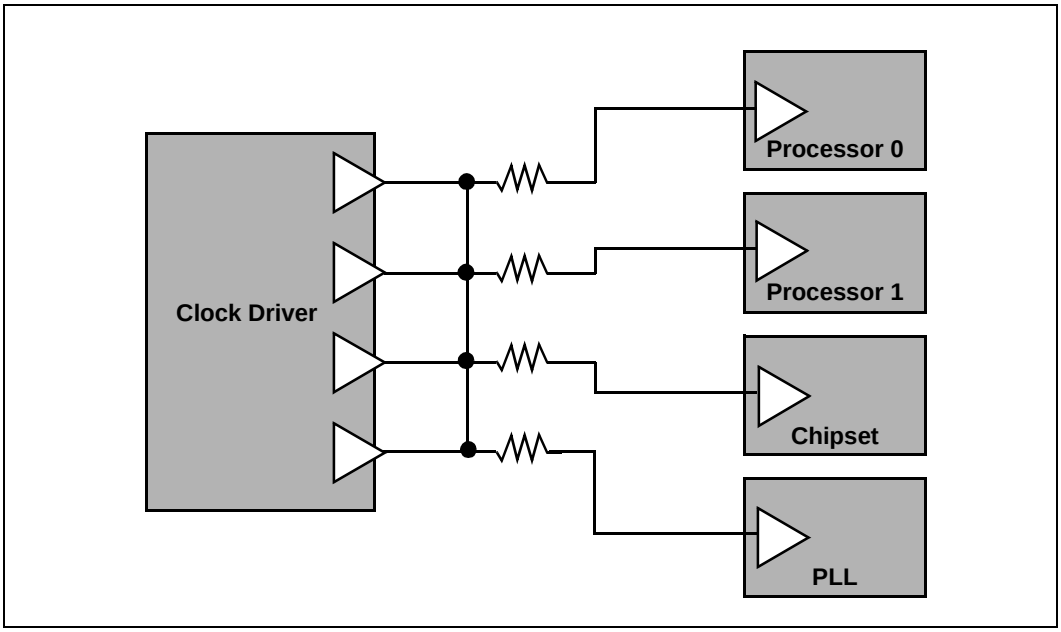
The host bus clock signals are critical signals in a platform design. The signal integrity and timing of these signals should be carefully evaluated and simulated.

In general, the following layout recommendations should be followed for the host bus clocks:

- It is recommended that system bus clocks be routed on the signal layer next to the ground layer (referenced to ground).
- It is strongly recommended that system bus clocks do not traverse multiple signal layers.
- System clock routing over power plane splits should be minimized.
- If necessary, grounded guard band traces can be routed next to clock traces to reduce crosstalk to other signals.

Figure 11 shows the host bus clocking connections that must be made in a LV Intel Pentium III processor 512K system. Detailed information regarding the routing, layout, and termination of the processor and chipset connections can be found in "Single Ended Host Bus Clocking Routing" on page 25. The debug port routing has special requirements and are provided in "Debug Port Host Clock Connection" on page 29.

Figure 11. Host Bus Clock Connections



The clocking requirements and timing information for the LV Intel Pentium III processor 512K can be found in the *Low Voltage Intel® Pentium® III Processor 512K Datasheet*. For additional information about the timing and clocking requirements of the chipset component, please contact your chipset vendor for the appropriate documentation.

4.2 Single Ended Host Bus Clocking Routing

LV Intel Pentium III processor 512K platforms support single-ended host bus clock drivers. When using this clocking method, the BCLK signal (ball AC1) is used as the single-ended clock input to the LV Intel Pentium III processor 512K. The BCLK#/CLKREF signal (ball AD1) is used as a reference voltage and must be connected to the appropriate filter circuit described in "CLKREF Filter Implementation" on page 27.

Figure 12 shows the topology that should be used for the LV Intel Pentium III processor 512K clock traces. Please note that L0, L1, and L2 refer to trace lengths between the illustrated components. Table 15 contains the recommended lengths and component values for this topology.

Figure 12. Single Ended Clocking Topology - CPU

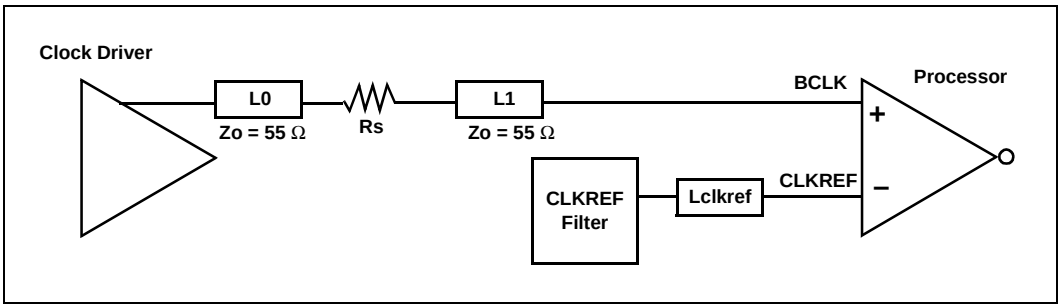


Figure 13 shows the topology that should be used for the chipset clock traces. Note that L*n* refers to trace lengths between the illustrated components. Table 15 contains the recommended lengths and component values for this topology.

Figure 13. Single Ended Clocking Topology

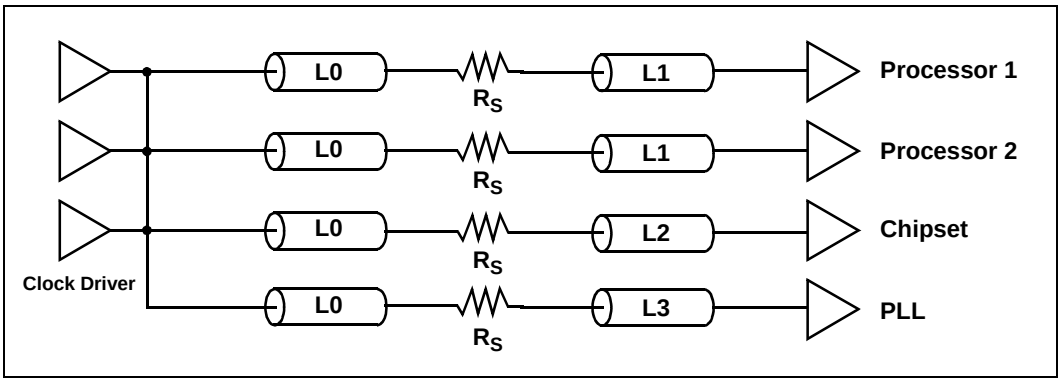


Table 15. Component Values for SE Clocking Topology

Reference	Value	Notes
L0	0.25” to 0.5”	You may flood this area
L1	5” to 9”	Match processor 0 and processor 1 L1 lengths as close as possible (maximum delta of 0.20”)
L2	L1 – 1.2”	
L3	L1 – 0.6”	L3 length may be adjusted depending on the clock chip vendor
Lclkref	0” – 1”	Minimize this trace length
Rs	22 to 33 Ω	1% Tolerance

The following guidelines should also be followed for single-ended clock implementations:

- BCLK must be routed through trace impedance of 55 Ω +/- 10%.
- Use 4 mil wide traces.
- Place all serial termination resistors within 0.50 inches to clock driver pins.
- Place all other signals at least 20 mils from the clock traces.
- All the termination resistors are rated at 1% accuracy.
- Match processor 0 and processor 1 L1 lengths as close as possible (maximum delta of 0.20”)

Note: The chipset may use a different clock reference level than the processor. This difference should be considered when determining clock routing trace lengths.

4.2.1 CLKREF Filter Implementation

When using single-ended clocking mode, the BCLK#/CLKREF signal on the LV Intel Pentium III processor 512K serves as a reference voltage to the clock input. To provide a steady reference voltage, a filter circuit must be implemented and attached to this pin. Figure 14 shows the recommended CLKREF filter implementation. The CLKREF filter should be placed as close as possible (less that 1.0 inch) to the processor's CLKREF pin.

Figure 14. CLKREF Filter Implementation

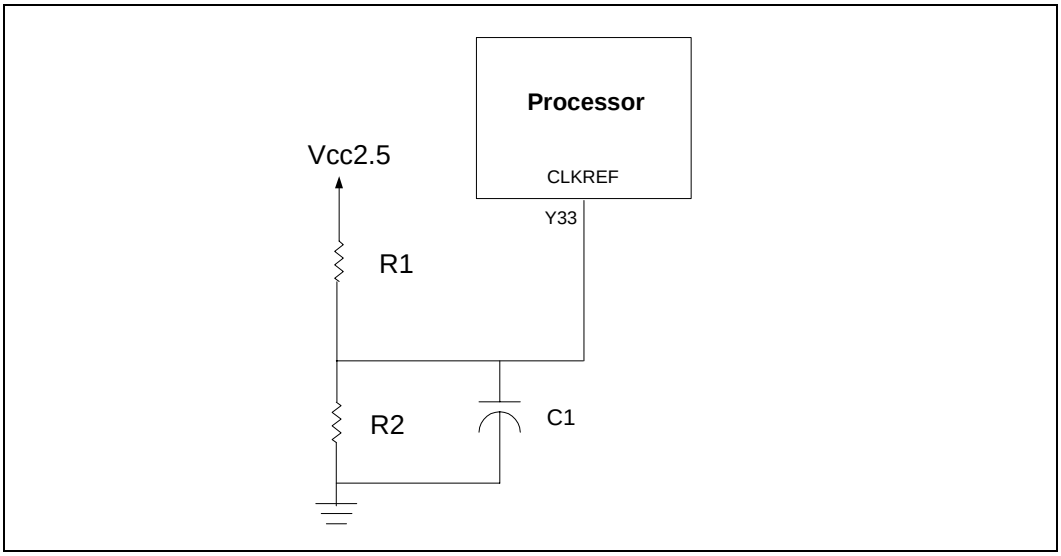


Table 16. CLKREF Component Values

Reference	Value	Notes
R1	150 Ω	1% Tolerance
R2	150 Ω	1% Tolerance
C1	4.7 µF	

4.2.2 Single-Ended Clocking BSEL[1:0] Implementation

In a LV Intel Pentium III processor 512K platform that uses single-ended (SE) clocking or a clock source that does not support the VTT_PWRGD protocol, the normal BSEL frequency selection process does not work. Since the clock generator is not compatible with dynamic BSEL assertions, all BSEL[1:0] signals should not be connected together. Instead, the BSEL pins on the clock generator should be pulled-up to 3.3 V through a 1 KΩ, 5% resistor. This strapping forces the clock generator into 133 MHz clocking mode and will only support 133 MHz capable processors. In addition, each BSEL[1:0] of each processor should be left unconnected. Figure 15 shows a diagram of this implementation.

Figure 15. Single-Ended Clock BSEL Circuit (133 MHz)

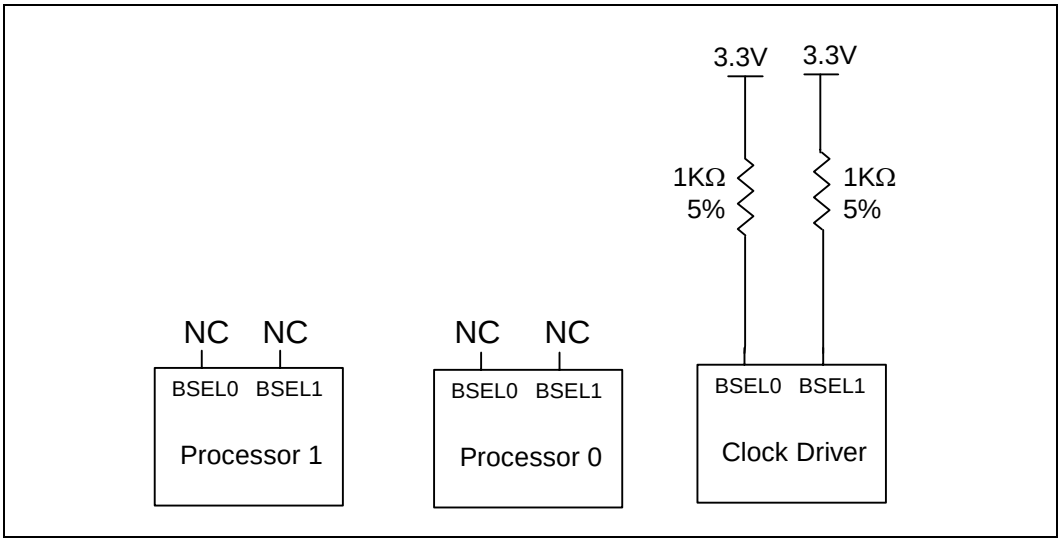


Table 17. BSEL[1:0] Encoding

BSEL[1:0]	System Bus Frequency
11	133 MHz

NOTE: All other BSEL[1:0] combinations are not supported.

4.3 Debug Port Host Clock Connection

In order to recover full front side bus speed BPM[5:0]# and RESET# data with the ITP, the Debug Port should be placed as close as is physically reasonable to the system bus, and no further than 1.5 ns flight time (as measured by trace length of the BPM[5:0]# and RESET# signals) from the nearest front side bus agent. System designers should record the flight time of the BPM[5:0]# and RESET# signals from the nearest front side bus agent to the Debug Port. This value will be important during the routing of several other Debug Port signals.

When BCLK and BCLK# (in differential clocked systems) signals are routed from the system clock buffer to each of the synchronous clock agents with a matched length, the copy of these signals from the system clock buffer to the ITP Debug Port must have a flight time equal to the matched length of the other synchronous clock agents plus the flight time of the BPM[5:0]# signals from the nearest bus agent to the Debug Port noted above. This ensures that the same BCLK to BPM[5:0]# phase relationship seen at the closest system bus agent will be present at the Debug Port pins. Clock trace lengths may be adjusted to center the recovery of BPM[5:0]# and RESET# at the Debug Port within the ITP receiver setup and hold window.

For a single-ended clock driver design, the topology illustrated in Figure 15 should be used. In this case, the “chipset” in the illustration is actually the debug port pin. The trace length L0 and the Rs value are the same as recommendations for the chipset in Table 15. However, the length of the trace segment L1 should be chosen so that it complies with the requirements described in the previous paragraph. This means that the L1 for the debug port is at least as long as the L1 for the processor clock traces.

4.4 Clock Driver Decoupling and Power Delivery

The decoupling and power delivery requirements of the system clock driver are dependent on the clock driver and chipset used in the system implementation. Because of this, no specific information can be provided in this document. However, since proper decoupling and noise-free power delivery are critical to the clock driver’s operation, Intel encourages system implementors to carefully follow the chipset and clock driver vendor’s recommendations in these areas. An incorrect implementation of these circuits can easily cripple a clock driver’s ability to produce reliable clock signals and lead to system instability. Please refer to the appropriate clock driver and chipset vendor information for more details.

5.0 Power

The intent of this section is to familiarize the reader with the processor power requirements for a LV Intel Pentium III processor 512K platform, and to show simulation model and power implementation techniques. Only specific power distribution and control issues pertaining to the LV Intel Pentium III processor 512K are discussed in this section. It is assumed that the reader is familiar with power distribution issues of the Intel® Pentium® III processors.

5.1 Terminology

"***Power-Good***" or "***PWRGOOD***" (an active high signal) indicates that all of the supplies and clocks within the system are stable. PWRGOOD should go active at a predetermined time after system voltages are stable and should go inactive as soon as any of these voltages fail their specifications.

"***VCC***" or "***Vcc_{CORE}***" refers to the LV Intel Pentium III processor 512K core's V_{CC} and cache supply voltage.

"***V_{TT}***" refers to the processor's I/O supply voltage.

"***AGTL***" refers to the processor's Assisted Gunning Transceiver Logic supply voltage. "AGTL" is the bus between the processor and its chipset. The terms "AGTL" and "system bus" are synonymous.

"***VRM 8.5***" refers to the voltage regulator for the LV Intel Pentium III processor 512K. It is a DC-DC converter that supplies the required voltage and current to each processor.

"***PLL1***" and "***PLL2***" are voltage supplies for the processor's PLL. These supplies must be filtered to provide a very clean voltage source.

5.2 Typical Power Delivery

Power distribution is generally thought of as *supplying power to the components that require it.* Digital designers typically assume that an ideal supply will be provided. The printed circuit board (PCB) designers attempt to create this ideal supply with two power planes in the PCB or by using large width traces to distribute power. High frequency noise created when logic gates switch is typically controlled with high frequency ceramic capacitors, which are recharged from lower frequency bulk capacitors. Various *rule of thumb* methods exist for determining the amount of each type of capacitance that is required. For LV Intel Pentium III processor 512K dual processor designs, the system designer needs to design beyond the rule of thumb and architect a power distribution system that meets LV Intel Pentium III processor 512K specifications. Figure 16 shows the ideal power model.

Figure 16. Ideal LV Intel® Pentium® III Processor 512K Power Supply Scheme

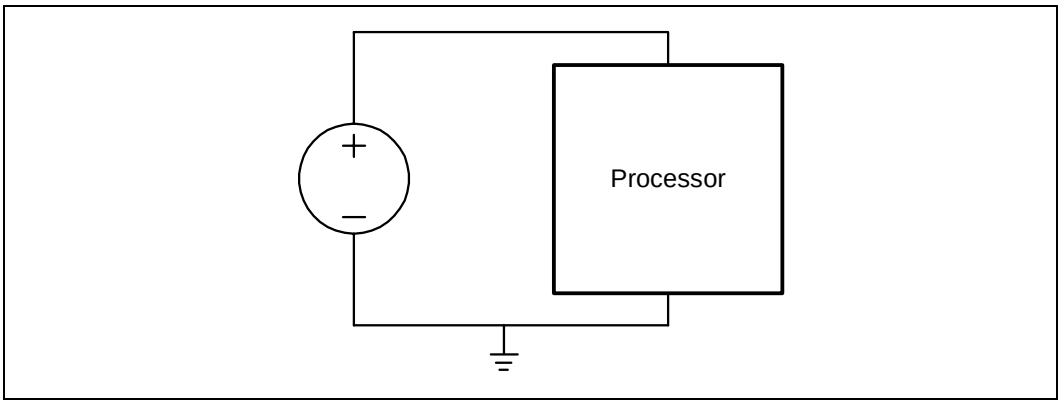
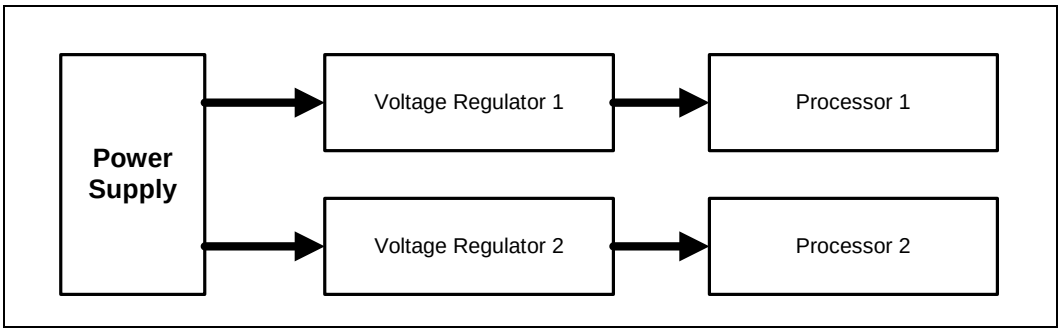


Figure 17 shows the recommended system baseboard solution involving local voltage regulators. It is recommended that board designers follow the guidelines in *VRM 8.5 DC-DC Converter Design Guidelines* (order number 249659).

Each regulator circuit should be placed as close as possible to the corresponding processor and aligned to the side of the socket with the higher density of power and ground pins.

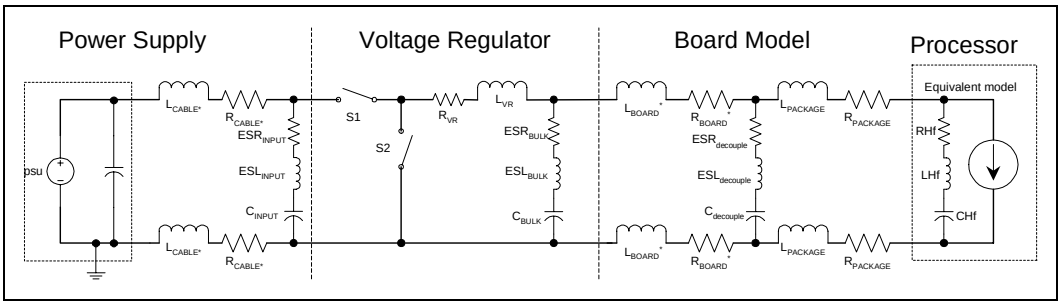
Important: In previous generation Pentium® III processor dual-processor systems, it was possible to source the combined voltage and current requirements for both processors from one large voltage regulator. **However, due to the load-line characteristics specified for the LV Intel® Pentium® III Processor 512K, Intel recommends that separate power planes be utilized**. This configuration of voltage regulators is shown in Figure 17.

Figure 17. Power Distribution for a DP System Motherboard



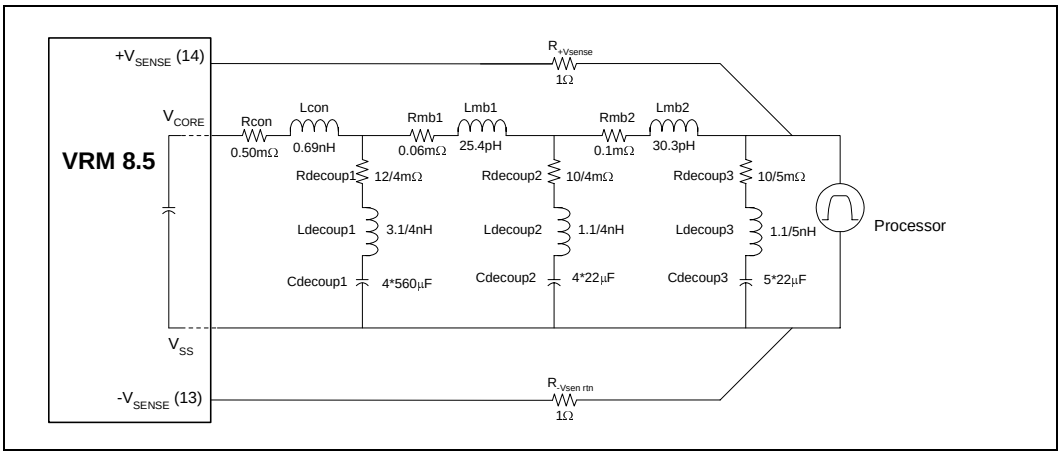
To completely model the motherboard system, the designer must include the inductance and resistance that exists in the cables, connectors, PCB planes, pins and body of components (such as resistors and capacitors), processor and voltage regulator. A more detailed model showing these effects is shown in Figure 18.

Figure 18. Detailed Power Distribution Model



The voltage regulator should be designed in conjunction with the recommended load model referenced in Figure 19.

Figure 19. VRM 8.5 Board Power Distribution Model



5.3 LV Intel® Pentium® III Processor 512K Power Requirements

This section describes the issues related to supplying power to the processor. For detailed electrical specifications, please refer to the *Low Voltage Intel® Pentium® III Processor 512K Datasheet*.

5.3.1 Voltage Tolerance

Refer to the *Low Voltage Intel® Pentium® III Processor 512K Datasheet* for voltage tolerance specifications. Failure to meet these specifications on the low-end tolerance results in transistors slowing down and not meeting timing specifications. Failure to meet the specifications on the high-end tolerance can cause damage or reduce the life of the processor.

5.3.2 Multiple Voltages

The VRM 8.5 voltage regulator, which provides the Vcc_{CORE} supply to the processor, can supply voltages from +1.05 V to +1.825 V. The VRM 8.5 voltage regulator can provide adequate power for all speed versions of the LV Intel Pentium III processor 512K. Refer to the *VRM 8.5 DC-DC Converter Design Guidelines* document for available voltage details.

Multiple voltages required for a dual processor system are Vcc_{CORE}, V_{REF}, V_{TT}, $Vcc_{CMOS1.5}$, and V_{SS}. Refer to the *Low Voltage Intel® Pentium® III Processor 512K Datasheet* document for the pin location of these voltages.

5.3.3 Voltage Sequencing

When designing a system with multiple voltages, there is always the issue of ensuring that no damage occurs to the system during voltage sequencing. Voltage sequencing is the timing relationship between two or more voltages. Sequencing applies to the power voltage levels and the levels of other crucial signals when the user turns the power supply on or off, or the system enters a failure condition. Systems should be designed such that neither supply stays on for extended time while the other is off. Excessive exposure to these conditions can compromise long-term component reliability.

For more information on the power-up sequence, refer to the *Low Voltage Intel® Pentium® III Processor 512K Datasheet*.

5.4 Meeting Dual Processor Power Requirements

Intel recommends that designers use a VRM 8.5 compliant regulator for LV Intel Pentium III processor 512K baseboard designs. Place high frequency and bulk decoupling capacitors as needed between the VRM 8.5 and the processor to ensure voltage fluctuations remain in specification.

The processor power supply design requires trade-offs between power supply, distribution and decoupling technologies. This section provides step by step instruction for designing a system that uses the more accurate power distribution model shown in Figure 18.

5.4.1 Supplying Voltage

Local (point of load) regulation is recommended for the LV Intel Pentium III processor 512K to satisfy the higher current requirements and to maintain power converter output voltage tolerance. For example, a DC-to-DC converter, placed close to the load, converts a higher DC voltage to a lower level using either a linear or switching regulator. Distributing lower current at a higher voltage to the converter minimizes unwanted losses (I x R) and localizes losses to the planes between the converter and the processor sockets.

It is recommended that voltage regulator solutions employ differential remote sense (as illustrated in Figure 19) to compensate for voltage drops between the regulators and the socket pins. The sense lines should be terminated as close to the center of the socket as possible and should not have an impedance greater than 1 Ω.

5.4.2 Decoupling Technology and Transient Response

Inductance of the system due to cables and power planes reduces the power supply's ability to respond quickly to a current transient. Decoupling a power plane can be characterized by several zones of interest. The closer to the load the capacitor is placed, the more inductance that is bypassed. By bypassing the inductance of leads, power planes, etc., less capacitance is required. However, closer to the load there is less room for capacitance. Therefore trade-offs must be made.

The LV Intel Pentium III processor 512K causes large switching transients. These sharp surges of current occur at the transition between low power mode and high power mode. It is the responsibility of the system designer to provide adequate high frequency decoupling to manage the

highest frequency components of the current transients. To lower total board inductance and resistance, the processor is designed with approximately 81 Vcc_{CORE} and 146 V_{SS} (ground) pins. Larger bulk storage (C_{BULK}), such as electrolytic (OSCON) capacitors, supply current during longer lasting changes in current demand by the component, such as coming out of an idle condition. Similarly, they act as a storage well for current when entering an idle condition from a running condition.

Power bypassing is required due to the relatively slow speed at which a DC-to-DC converter can react. The loop response time of the converter feedback circuit is much longer than the time it takes a processor load change to take effect. This is especially true if the processor load changes are happening at a high rate. Bulk capacitance supplies energy from the time the high frequency decoupling capacitors are drained until the power supply can react to the demand. More correctly, the bulk capacitors in the system slow the transient requirement seen by the power source to a rate that it is able to supply, while the high frequency capacitors slow the transient requirement seen by the bulk capacitors to a rate that they can supply.

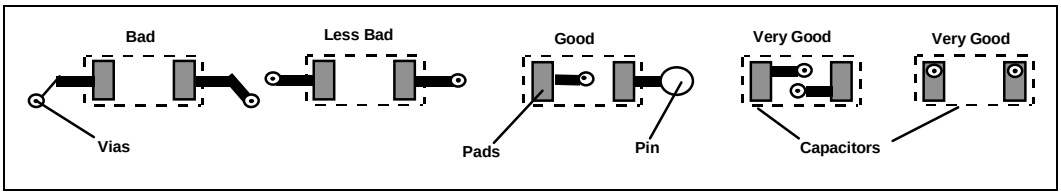
A load-change transient occurs when coming out of or entering a low power mode. These are not only quick changes in current demand, but are also long lasting average current requirements. Maintaining voltage tolerance during these changes in current requires high-density bulk capacitors with low Effective Series Resistance (ESR) and low Effective Series Inductance (ESL). Use thorough analysis when choosing these components.

5.4.2.1 Location of High-Frequency Decoupling

A system designer for the LV Intel Pentium III processor 512K should properly design for high-frequency decoupling. High-frequency decoupling should be placed as close to the power pins of the processor as physically possible. If necessary, use both sides of the board for placing components; this will achieve the optimum proximity to the power pins. This is vital, since the inductance of the board's metal plane layers could cancel the usefulness of these low inductance components.

Another method to lower the inductance that should be considered is to shorten the path from the capacitor pads to the pins that it is decoupling. If possible, place the vias connecting to the planes within the pad of the capacitor. If this is not possible, keep the traces as short and wide as is feasible. Possibly one or both ends of the capacitor can be connected directly to the pin of the processor without the use of a via. Even if simulation results look good, these practical suggestions can be used to create an even better decoupling situation where they can be applied in layout. Figure 20 illustrates these concepts.

Figure 20. 1206 Capacitor Pad and Via Layouts



5.4.2.2 Location of Bulk Decoupling

The location of bulk capacitance is not as critical as the high frequency decoupling components. Careful placement is still important for these components to minimize the effects of parasitic board impedances impacting transient response capability. Further, location and component impedances are useful in simulation of the power conversion circuit. Bulk components should be placed close to the processor sockets to minimize AC delays.

Note that bulk capacitors on voltage regulators are effectively electrically located behind the inductance of the converter pins. As a result bulk capacitors need to be utilized close to the processor socket.

The recommended number of bulk decoupling components and board load model for use with voltage regulators is illustrated in Table 18 and Figure 19.

Table 18. LV Intel Pentium III processor 512K Bulk Capacitance Recommendations

Design Type	Bulk Capacitance	ESR	ESL	RMS Current Rating
On-board design	4 OSCON, 560 µF	12 mΩ	3.1 nH max	5.04 A rms

5.5 Recommendations

Intel recommends using simulation to design and verify LV Intel Pentium III processor 512K systems. With the estimates provided in the previous section, a model of the power source, and the model of the processor, system developers can begin analog modeling. The following sections contain Intel's design recommendations.

5.5.1 Decoupling Guidelines for LV Intel® Pentium® III Processor 512K Designs

5.5.1.1 Decoupling Guidelines

The processor's Micro-FCBGA package has eight surface mount decoupling capacitors. Six 0.68-µF capacitors are on V_{CC} and two 0.68-µF capacitors are on V_{TT}. In addition to the package capacitors, sufficient board level capacitors are also necessary for power supply decoupling. These guidelines are as follows:

- High and Mid Frequency V_{CC} decoupling – Place twenty-four 0.22-µF X5R 0603 capacitors directly under the package on the solder side of the motherboard using at least two vias per capacitor node. Ten 10-µF X7R 6.3V 1206-size ceramic capacitors should be placed around the package periphery near the balls. Trace lengths to the vias should be designed to minimize inductance. Avoid bending traces to minimize ESL.
- High and Mid Frequency V_{TT} decoupling – Place ten 1-µF X7R 0603 ceramic capacitors close to the package. Via and trace guidelines are the same as above.
- Bulk V_{CC} decoupling – Minimum of 1200 µF capacitance with equivalent series resistance less than or equal to 3.5 mΩ.

5.5.1.2 AGTL V_{REF} Decoupling Design

Three 0.1-µF capacitors in 0603 packages should be placed within 500 mils of the V_{REF} pins. Two should be connected between V_{TT} and V_{REF}, and one should be connected between V_{REF} and ground. If this circuit is far from the processor, add a 0.1-µF capacitor for decoupling.

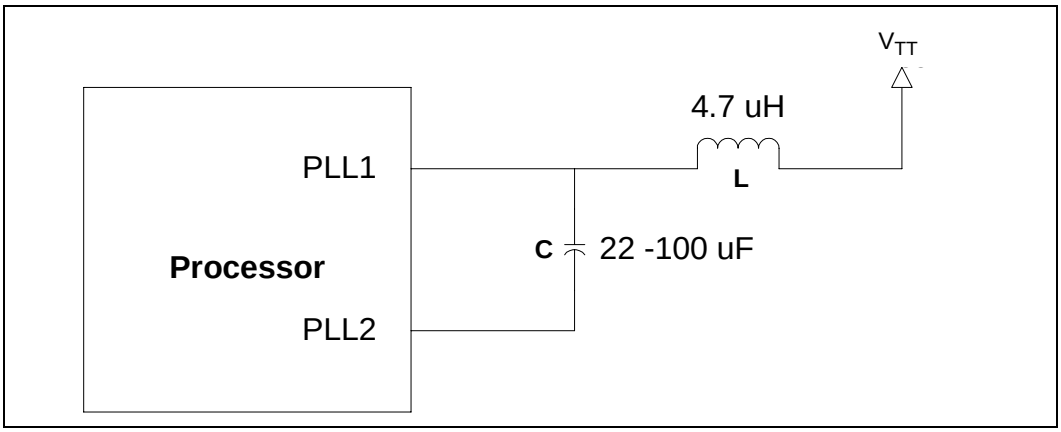
5.5.2 PLL Filter Recommendations

It is highly critical that phase lock loop power delivery to the processor meets Intel's requirements. A low pass filter is required for power delivery to pins PLL1 and PLL2. This serves as an isolated, decoupled power source for the internal PLL.

5.5.2.1 Topology

The LV Intel Pentium III processor 512K has internal phase lock loop (PLL) clock generators, which are analog and require a quiet power supply to minimize jitter. PLL1 should have a 4.7-µH inductor connected in series to V_{TT}, and PLL2 should be connected through a capacitor (22- to 100-µF) to PLL1. See Figure 21.

Figure 21. Processor PLL Filter



Other routing requirements:

- The capacitor (C) should be close to the PLL1 and PLL2 pins, < 0.1Ω per route.
- The PLL2 route should be parallel and next to PLL1 route (minimize loop area).
- The inductor (L) should be close to C; any routing resistance should be inserted between V_{TT} and L.

5.5.2.2 Filter Specification

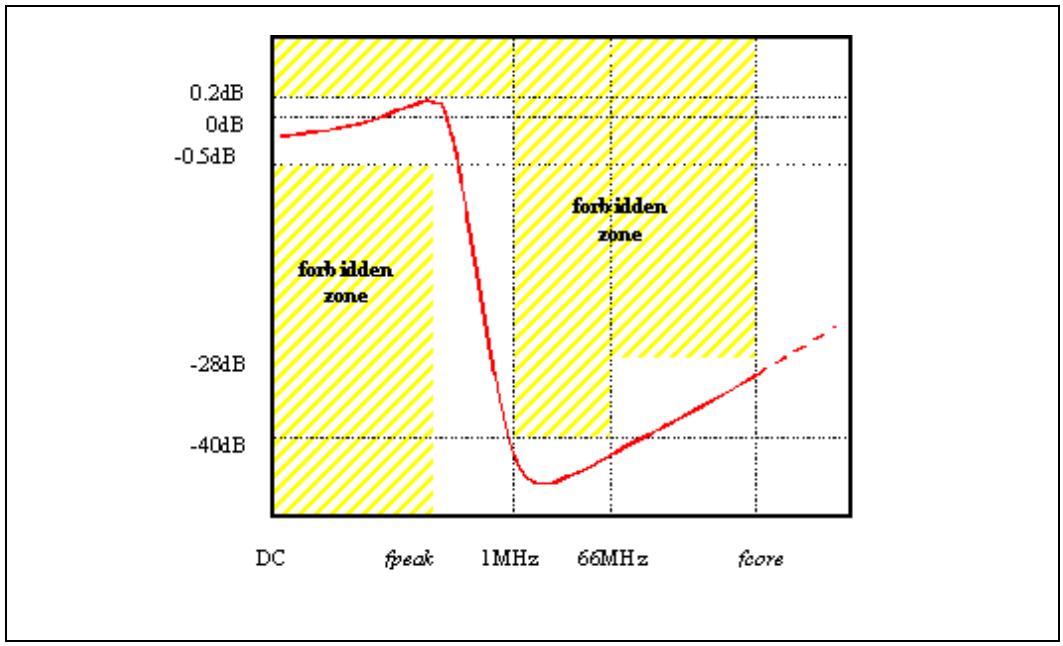
The function of the filter is to protect the PLL from external noise through low-pass attenuation.

The low-pass specification, with input at V_{TT} and output measured across the capacitor, is as follows:

- < 0.2 dB gain in pass band
- < 0.5 dB attenuation in pass band (see DC drop in next set of requirements)
- > 34 dB attenuation from 1 MHz to 66 MHz
- > 28 dB attenuation from 66 MHz to core frequency

The filter specification is shown in Figure 22.

Figure 22. PLL Power Low Pass Filter Response



Other requirements:

- Use shielded type inductor to minimize magnetic pickup
- Filter should support DC current > 30 mA
- DC voltage drop from V_{TT} to PLL1 should be < 60 mV, which in practice implies series R < 2 Ω. It also means pass band (from DC to 1Hz) attenuation is < 0.5 dB for VCC = 1.1 V, and < 0.35 dB for VCC = 1.5 V.

6.0 Thermals

The LV Intel Pentium III processor 512K requires a robust thermal solution for proper operation. Please refer to the *Low Voltage Intel® Pentium III Processor 512K (DP) Thermal Design Guide* for more information.

6.1 THERMTRIP# Requirements

In the event the processor drives the THERMTRIP# signal active during valid operation, both the Vcc and Vtt supplies to the processor must be powered off to prevent thermal runaway of the processor. Valid operation refers to operating conditions in which the THERMTRIP# signal is guaranteed valid. The time required from THERMTRIP# assertion to V_{CC} rail at 1/2 nominal is 5 seconds; the time required from THERMTRIP# assertion to V_{TT} rail at 1/2 nominal is 5 seconds.

Table 19. THERMTRIP# Timing Requirements

Power Rail	Power Target	Time Required for Power Drop
V_{CC}	1/2 Nominal V_{CC}	5.0 seconds
V_{TT}	1/2 Nominal V_{TT}	5.0 seconds

6.2 THERMTRIP# Erratum

Intel has identified an issue with THERMTRIP# which may incorrectly assert during de-assertion of RESET# at nominal operating temperatures in LV Intel Pentium III processor 512K A-1 stepping processors. The assertion of THERMTRIP# with cause the processor to shut down internally and stop execution. This issue can lead to intermittent system power-on boot failures.

To prevent the risk of power-on boot failures a platform workaround is required. The system must provide a rising edge on the TCK signal during the power-on sequence that meets all of the following requirements:

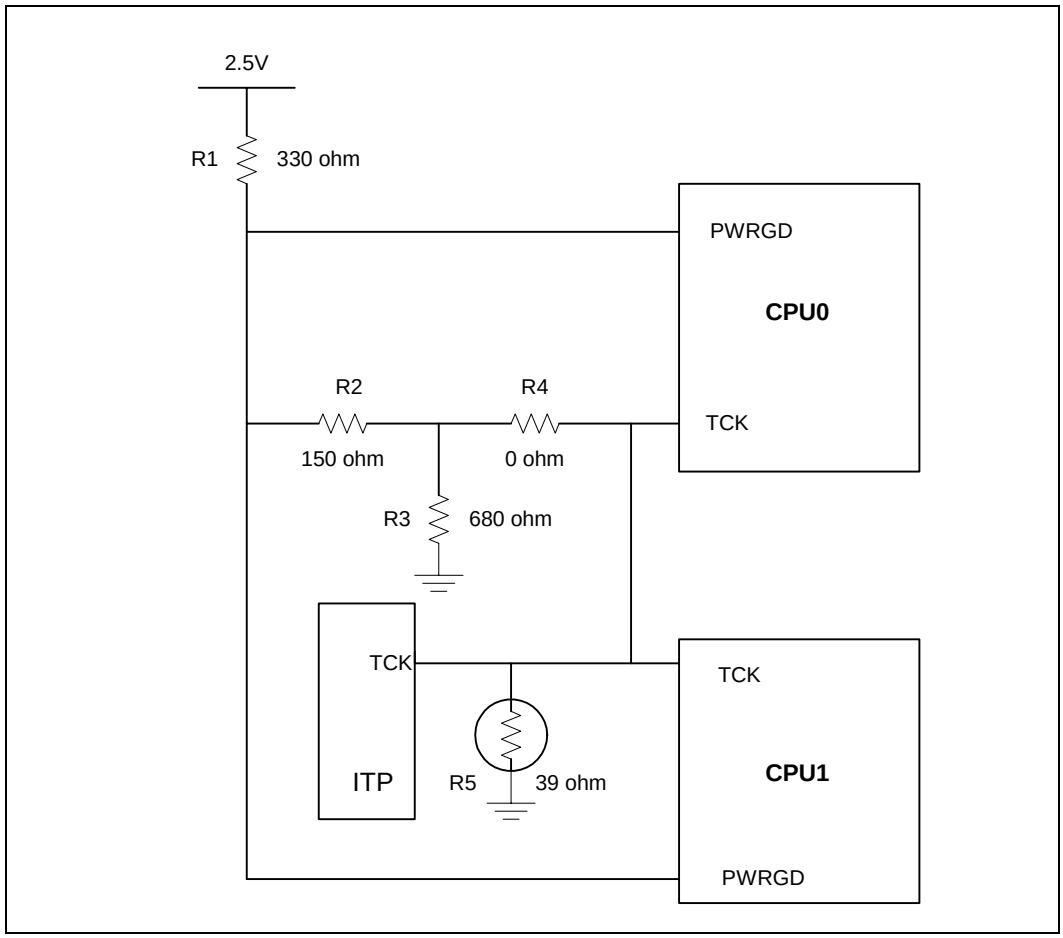
- Edge occurs after Vcc_{CORE} is valid and stable
- Edge occurs before or at the de-assertion of RESET#
- Edge occurs after all V_{ref} input signals are at valid voltage levels
- TCK input meets the Vih_{min} and Vih_{max} spec requirements of the *Low Voltage Intel® Pentium® III Processor 512K Datasheet.*

Specific workaround implementations may be platform specific. The following example has been tested as a acceptable workaround implementation.

The example workaround circuit, shown in Figure 23, requires circuit modifications for ITP tools to function correctly. These modifications must remove the workaround circuitry from the platform and may cause systems to fail to boot. Issuing the ITP 'Reset Target' command on failing systems will reset the system while providing a sufficient rising edge on the TCK pin to ensure system boot.

The example workaround circuit (shown in Figure 23) does not support production motherboard test methodologies that require the use of the processor JTAG/TAP port. Alternative workaround solutions must be found if such test capability is required.

Figure 23. LV Intel Pentium III processor 512K Example THERMTRIP# Workaround Circuit



NOTES:
1. For Production Boards: Depopulate R5
2. To use ITP: Install R5, Depopulate R4
3. Assumes the inputs to the CPU_PWRGD are open collector signals that are Wire-ANDed together

The example workaround circuit assumes that the PWRGD inputs into the processors are open collector. Tying the PWRGD inputs together in a Wired-AND fashion allows each processor to receive PWRGD at the same time but at the latter of the 2 separate PWRGD assertions. When separation of the PWRGD inputs to each processor is required, extra circuitry is required.

Please consult the *Pentium® III Processor Specification Update* (order number 244453) for additional information on this issue.

7.0 System Design Checklist

7.1 Introduction

This checklist highlights design considerations that should be reviewed prior to manufacturing a motherboard that implements a LV Intel Pentium III processor 512K system design. This is not a complete list and does not guarantee that a design will function properly.

The following tables contain design considerations for the various portions of a design. Each table describes one portion and is titled accordingly.

7.2 Host Interface AGTL Bus and AGTL Signals

It is strongly recommended that AGTL signals be routed on signal layers next to the ground layer. It is important to provide effective signal return paths with low inductance.

Table 20. AGTL Signals (Sheet 1 of 2)

CPU Pin	Pin Connection
A[35:3]#	Connect to chipset and second CPU.
ADS# (AA3)	Connect to chipset and second CPU.
AERR# (W2)	Connect to chipset and second CPU. Pull up to VTT through a 150 Ω resistor at the chipset. See “Wired-OR Signal Considerations” on page 15 for details.
AP[1:0]#	Connect to chipset and second CPU.
BERR# (C14)	Connect to chipset and second CPU. Pull up to VTT through a 150 Ω resistor at the chipset. See “Wired-OR Signal Considerations” on page 15 for details.
BINIT# (AF23)	Connect to chipset and second CPU. Pull up to VTT through a 150 Ω resistor at the chipset. See “Wired-OR Signal Considerations” on page 15 for details.
BNR# (L2)	Connect to chipset and second CPU. Pull up to VTT through a 150 Ω resistor at the chipset. See “Wired-OR Signal Considerations” on page 15 for details.
BP[3:2]#	Leave as N/C.
BPM[1:0]	Leave as N/C.
BPRI# (R2)	Connect to chipset and second CPU.
BR0# (A7)	Connect BR0# from CPU0 to BR1# of CPU1. Connect BR0# of CPU0 to BR0# of chipset.
BR1# (C4)	Connect BR1# from CPU0 to BR0# of CPU1.
D[63:0]#	Connect to chipset and second CPU.
DBSY# (W3)	Connect to chipset and second CPU.
DEFER# (T3)	Connect to chipset and second CPU.
DEP[7:0]#	Connect to chipset and second CPU.
DRDY# (Y1)	Connect to chipset and second CPU.
HIT# (AA2)	Connect to chipset and second CPU. Pull up to VTT through a 150 Ω resistor at the chipset. See “Wired-OR Signal Considerations” on page 15 for details.
HITM# (U2)	Connect to chipset and second CPU. Pull up to VTT through a 150 Ω resistor at the chipset. See “Wired-OR Signal Considerations” on page 15 for details.

Table 20. AGTL Signals (Sheet 2 of 2)

CPU Pin	Pin Connection
LOCK# (V3)	Connect to chipset and second CPU.
REQ[4:0]#	Connect to chipset and second CPU.
RESET# (B15)	Terminate to V_{TT} to match AGTL trace impedance which is typically 68 Ω, connect to chipset. For ITP, connect to pin 2 (RESET#) of ITP through a 240 Ω series resistor; terminate to V_{TT} to match AGTL trace impedance which is typically 68 Ω. Refer to Figure 9 for details.
RP# (T4)	Connect to chipset and second CPU.
RS[2:0]#	Connect to chipset and second CPU.
RSP# (M5)	Connect to chipset and second CPU.
TRDY# (W1)	Connect to chipset and second CPU.

7.3 CMOS (Non-AGTL) Signals

It is recommended to route CMOS signal traces on one signal layer, and not next to AGTL traces. Try to avoid long traces to eliminate speed path issues, especially for APIC clock and APIC data signals.

Table 21. CMOS Signals (Sheet 1 of 2)

CPU Pin	Pin Connection
A20M# (AC3)	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic. For boards supporting preproduction processors, this pin must be connected to frequency selection circuitry.
FERR# (AF6)	Connect to second CPU and pull up through ~150 Ω to VccCMOS. May need to connect to chipset or server management logic.
FLUSH# (AF5)	Connect to second CPU and pull up through ~150 Ω to VccCMOS
IERR# (AF4)	Pull up through ~150 Ω to VccCMOS if connected to external logic. Leave unconnected otherwise.
IGNNE# (AD9)	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic. For boards supporting preproduction processors, this pin must be connected to frequency selection circuitry.
INIT# (AE6)	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic.
LINT0/INTR (AD15)	Connect to interrupt control logic and second CPU and pull up through ~330 Ω to VccCMOS. For boards supporting preproduction processors, this pin must be connected to frequency selection circuitry.
LINT1/NMI (AE14)	Connect to interrupt control logic and second CPU and pull up through ~330 Ω to VccCMOS. For boards supporting preproduction processors, this pin must be connected to frequency selection circuitry.
PICD[1:0]	Connect to second CPU and pull up through ~150 Ω to VccCMOS. May also need to be connect to interrupt control logic.
PWRGOOD (AB4)	Connect to second CPUs and pull up through 150-330 Ω to 1.8 V output from the PWRGOOD logic.
SLP# (AF8)	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic.

Table 21. CMOS Signals (Sheet 2 of 2)

CPU Pin	Pin Connection
SMI# (AD3)	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic.
STPCLK# (AE4)	Connect to second CPU and pull up through ~330 Ω to VccCMOS. May also need to be connected to chipset or compatibility logic.
THERMTRIP# (AE10)	See “Thermals” on page 38 for details

7.4 TAP/ITP Checklist

There are several mechanical, electrical, and functional constraints on the debug port which must be followed; see the *Low Voltage Intel® Pentium® III Processor 512K Datasheet*.

Table 22. TAP/ITP Signals

CPU Pin	Pin Connection
PRDY# (AE22)	Pull-up resistor that matches GTL characteristic impedance to VTT, 240 Ω series resistor to ITP.
PREQ# (AF19)	200-300 Ω pull-up to VccCMOS and connect to ITP.
TCK (AD10)	Connect to other CPU, then to 39 Ω pull-down to Gnd, and connect to ITP.
TDO (AD11)	150 Ω pull-up to VccCMOS and connect to ITP from CPU0.
TDI (AD7)	200-300 Ω pull-up to VccCMOS and connect to ITP. Connect TDI from CPU0 to TDO on CPU1.
TMS (AF7)	Connect to other CPU, then to 39 Ω pull-up to VccCMOS and connect to ITP.
TRST# (AF15)	Connect to other CPU, then to 500-680 Ω pull-down to Gnd and connect to ITP.

7.5 Miscellaneous Checklist

Host bus clocks are critical. Signal integrity and timing of these signals should be carefully evaluated and simulated. Intel strongly recommends that system bus clocks be routed on signal layers next to the ground layer and that they do not traverse multiple signal layers.

Table 23. Clock Signals

CPU Pin	Pin Connection
BCLK (AC1) BCLK#/CLKREF (AD1)	For single ended clocking connect BCLK to Clock Generator through 22 - 33 Ω series resistor (OEM must simulate based on driver characteristics). Connect BCLK# to a filtered 1.25 V supply.To reduce pin-to-pin skew, tie host clock outputs together at the clock driver, then route to both processors and chipset.
PICCLK (AF20)	Must be connected from the clock generator to the PICCLK pin on the CPUs. Voltage divider circuitry should yield 2.0 V (OEM must simulate based on driver characteristics).

Table 24. Miscellaneous Signals

<table>
<tr><th>CPU Pin</th><th>Pin Connection</th></tr>
<tr><td>BSEL0 (AE12)
BSEL1 (AF10)</td><td>The table below shows the encoding scheme for BSEL[1:0]. The only supported system bus frequency for the LV Intel® Pentium® III Processor 512K (1.15 V) is 133 MHz. If another frequency is used, the processor is not guaranteed to function properly.
<table>
<tr><th>BSEL[1:0]</th><th>System Bus</th><th>Pin Connection</th></tr>
<tr><td>11</td><td>133 MHz</td><td>For single ended clocking pull both signals up to 3.3 V with a 1 KΩ resistor at the clock generator. NC on processor 0 and 1.</td></tr>
</table>
See Figure 15 for details.</td></tr>
<tr><td>THERMDN (AF14)</td><td>Thermal diode cathode. Connect to thermal sensor device.</td></tr>
<tr><td>THERMDP (AF13)</td><td>Thermal diode anode. Connect to thermal sensor device.</td></tr>
<tr><td>NCHCTRL (AD16)</td><td>Connect to V_{TT} through a 14 Ω 1% resistor.</td></tr>
<tr><td>RTTCTRL (AE16)</td><td>68 Ω 1% pull-down to GND.</td></tr>
<tr><td>SLEWCTRL (AF16)</td><td>110 Ω 1% pull-down to GND.</td></tr>
<tr><td>VID[3:0]</td><td>Each VID line must be pulled up to 3.3 V through a 1 KΩ resistor. These resistors can be either internal to the voltage regulator controller or placed externally on the motherboard.</td></tr>
<tr><td>VID25 (R3)</td><td>Each VID line must be pulled up to 3.3 V through a 1 KΩ resistor. These resistors can be either internal to the voltage regulator controller or placed externally on the motherboard.</td></tr>
</table>

Table 25. Power Signals

CPU Pin	Pin Connection
TESTHI[2:1]	Connect individually to V_{TT} through a 1 KΩ pull-up resistor.
TESTLO[2:1]	Connect to Ground through a 1 KΩ pull-down resistor.
PLL1, PLL2	Low pass filter on V_{TT} provided on the system board. Typically a 4.7 µH inductor in series with V_{TT} is connected to PLL1 then through a series 22-100 µF capacitor to PLL2.
Reserved	The following pins must be left as no-connects: A2, A5, A11, B1, C1, C22, D1, D26, E1, F1, L5, N4, N24, P1, P4, P5, P26, AD4, AD13, AD23, AE8, AF17, AF18
Vcc_{CORE}	Connect to core voltage regulator. Provide low frequency decoupling. Guidelines: Place twenty-four 0.22-µF X5R 0603 capacitors directly under the package on the solder side of the motherboard using at least two vias per capacitor node. Ten 10-µF X7R 6.3 V 1206-size ceramic capacitors should be placed around the package periphery near the balls. Trace lengths to the vias should be designed to minimize inductance. Avoid bending traces to minimize ESL.
VREF[7:0]	Connect to Vref voltage divider made up of 75 Ω 1% and 150 Ω 1% resistors connected to V_{TT}. Processor VREF must be separate from Chipset VREF. Guidelines: Three each (minimum) 0.1 µF in 0603 package placed within 500 mils of VREF pins.
VCMOS_REF	Use 75 Ω/150 Ω resistor divider network to create a 1.0 V V_{CMOS_REF} value derived from V_{CC_CMOS}.
VTT_ PWRGOOD	Connected to V_{TT} through a 1 KΩ pullup resistor, and connect to VttPWRGOOD circuitry.
V_{TT}	Connect A26, C5, C7, C9, C11, C13, C15, C17, C19, C21, D5, E4, E6, G4, G23, J4, J23, L4, L23, N23, R23, U23, V4, W23, AA4, AA23, AC4, AC23, AD6, AD8, AD12, AD14, AD18, AD20, AE3, AE18, AF1, AF2 to 1.25 V regulator. Provide high and low frequency decoupling. Guidelines: Place ten 1-µF X7R 0603 ceramic capacitors close to the package. Via and trace guidelines are the same as above.